# ESP32-S Specification

Version V1

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CONTENT

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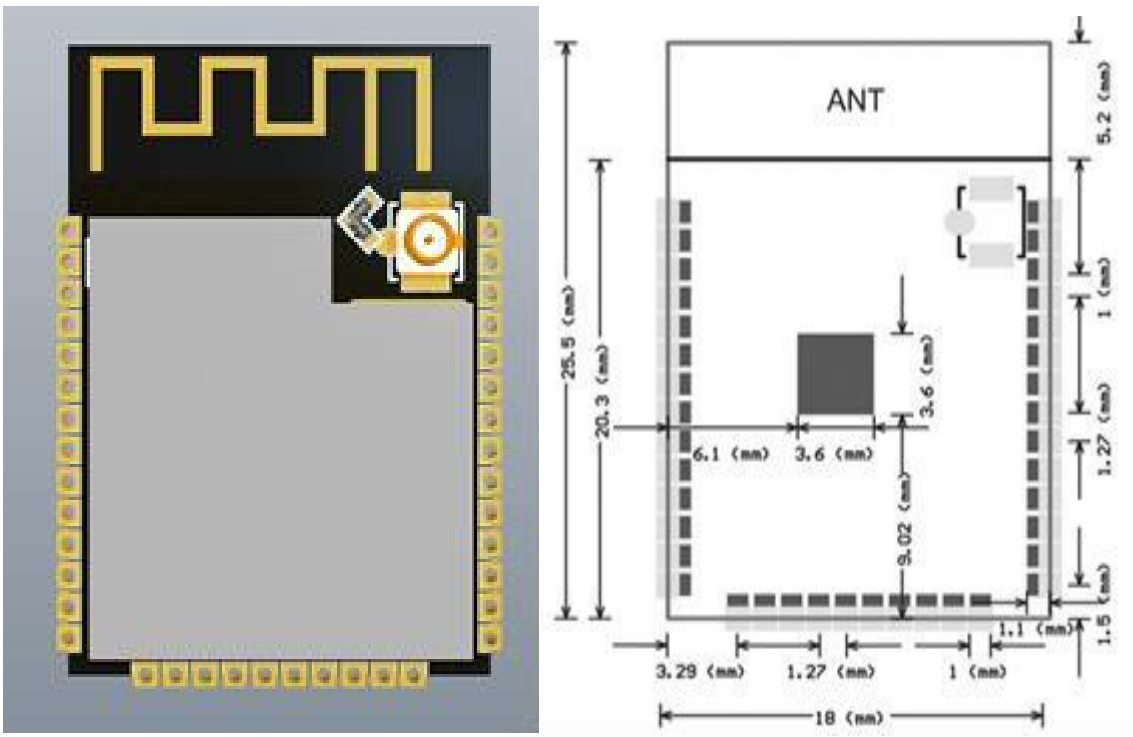
# 1. Product overview

ESP32-S is a general-purpose WiFi-BT-BLE MCU module with powerful functions and a wide range of uses. It can be used for low-power sensor networks and demanding tasks, such as voice encoding, audio streaming, and MP3 decoding.

The core of this module is the ESP32 chip, which is scalable and adaptive. The two CPU cores can be individually controlled or powered on. The user can cut off the power of the CPU and use the low-power coprocessor to continuously monitor the status changes of the peripherals or whether certain analog quantities exceed the threshold. ESP32 also integrates a wealth of peripherals, including capacitive touch sensors, Hall sensors, low-noise sensor amplifiers, SD card interface, Ethernet interface, high-speed SDIO/SPI, UART, I2S and I2C. The ESP32-S module was developed by Ai-Thinker Technology. The core processor ESP32 of this module has two built-in low-power Xtensa®32-bit LX6 MCUs. The main frequency supports 80 MHz, 160 MHz and 240 MHz.

**Appearance size**



## Characteristics

- Ultra-small 802.11b/g/n Wi-Fi + BT SoC module
- Adopt low-power dual-core 32-bit CPU, can be used as an application processor
- The main frequency is up to 240MHz, and the computing power is up to 600DMIPS
- Build-in 520KB SRAM
- Support interface of UART/SPI/I2C/PWM/ADC/DAC
- SMD-38 package, convenient for soldering and testing
- Support OpenOCD debugging interface
- Support multiple sleep modes, the minimum deep sleep current can reach 6.5 μA
- Support STA/AP/STA+AP working mode
- Support Smart Config/AirKiss one-click network configuration
- General AT commands can be used quickly
- Support serial port local upgrade and remote firmware upgrade (FOTA) embedded Lwip and FreeRTOS

## Main parameters

**Table 1.1 main parameters instruction**

| | |
|---|---|
| Model | ESP32-S |
| Package | SMD-38 |
| Size | 18.0*25.5*3.0（±0.2）mm |
| Certification | SRCC、FCC、CE、RoHS |
| SPI Flash | Default 32Mbit，maximum support 128Mbit |
| Interface | UART、SPI、SDIO、I2C、PWM、I2S、IR、ADC、DAC |
| IO | 22 |
| UART rate | Support 300 ~ 4608000 bps , default 115200bps |
| Bluetooth | Bluetooth 4.2 BR/EDR and BLE stander |
| Wi-Fi | 802.11 b/g/n/e/i |
| On-chip sensors | Hall sensor、Temperature sensor、Capacitive touch sensor |
| Spectrum range | 2412 ~2484MHz |
| Antenna | On-board PCB antenna/ IPEX |
| Transmit power | 802.11b: 17±2 dBm (@11Mbps)<br>802.11g: 14±2 dBm (@54Mbps)<br>802.11n: 13±2 dBm (@MCS7) |
| Receiving sensitivity | CCK, 1 Mbps : -90dBm<br>CCK, 11 Mbps: -85dBm<br>6 Mbps (1/2 BPSK): -88dBm<br>54 Mbps (3/4 64-QAM): -70dBm<br>MCS7 (65 Mbps, 72.2 Mbps): -67dBm |
| Power consumption (typical value) | Active (RF work) Wi-Fi Tx packet 13dBm~21dBm 160~260mA<br>Wi-Fi/BT Tx packet 0dBm 120mA<br>Wi-Fi/BT Rx and listening 80~90mA<br>Associated sleep patterns 0.9mA@DTIM3，<br>(Associated with Light-sleep mode)<br>1.2mA@DTIM1 Modem-sleep CPU is working<br>status Maximum speed：20mA<br>Normal speed：<br>5~10mA slow：<br>3mA<br>Light-sleep - 0.8mA<br>Deep-sleep ULP coprocessor is working 0.5mA<br>Ultra-low power sensor monitoring method25uA@1% duty<br>RTC timer + RTC memory 20uA<br>Hibernation Only the RTC timer is working 2.5uA |
| Security | WPA/WPA2/WPA2-Enterprise/WPS |

| | |
|---|---|
| Power supply range | Supply voltage 3.0V ~ 3.6V， Supply current >500mA |
| Operating temperature | -20 ℃ ~ 85℃ |
| Storage environment | -40 ℃ ~ 85℃ , < 90%RH |
| Weight | About 1.45g |

# 2.Pin definition

ESP32-S module is connected to 38 interfaces, table 2.1 and table 2.2 is the interface definition.

table 2.1 ESP32-S Pin diagram

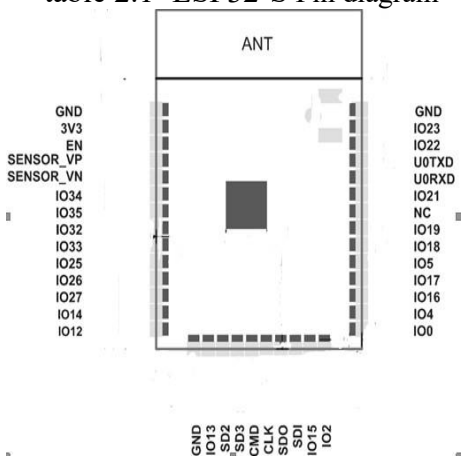



table 2.2 pin function definition

| No. | Pin | Function Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | 3V3 | 3.3V power supply(VDD)； The output current of the external power supply is recommended to be above 500mA |
| 3 | EN | Chip enable terminal, active at high level |
| 4 | SENSOR_VP | GPI36,SENSOR_VP,ADC_H,ADC1_CH0,RTC_GPIO0 |
| 5 | SENSOR_VN | GPI39,SENSOR_VN,ADC1_CH3,ADC_H,RTC_GPIO3 |
| 6 | IO34 | GPI34,ADC1_CH6,RTC_GPIO4 |
| 7 | IO35 | GPI35,ADC1_CH7,RTC_GPIO5 |
| 8 | IO32 | GPIO32,XTAL_32K_P(32.768kHz crystal oscillator input ADC1_CH4, TOUCH9,RTC_GPIO9 |
| 9 | IO33 | GPIO33,XTAL_32K_N(32.768kHz crystal oscillator output ADC1_CH5, TOUCH8,RTC_GPIO8 |
| 10 | IO25 | GPIO25,DAC_1,ADC2_CH8,RTC_GPIO6,EMAC_RXD0 |
| 11 | IO26 | GPIO26,DAC_2,ADC2_CH9,RTC_GPIO7,EMAC_RXD1 |
| 12 | IO27 | GPIO27,ADC2_CH7,TOUCH7,RTC_GPIO17,EMAC_RX_DV |

| | | |
|---|---|---|
| 13 | IO14 | GPIO14,ADC2_CH6,TOUCH6,RTC_GPIO16,MTMS, |
| | | HSPICLK,HS2_CLK,SD_CLK,EMAC_TXD2 |
| 14 | IO12 | GPIO12,ADC2_CH5,TOUCH5,RTC_GPIO15,MTDI,HSPIQ,HS2_DATA2,SD_DAT A2,EMAC_TXD3 |
| 15 | GND | Ground |
| 16 | IO13 | GPIO13,ADC2_CH4,TOUCH4,RTC_GPIO14,MTCK,HSPID,HS2_DATA3,SD_DAT A3,EMAC_RX_ER |
| 17 | SHD/SD2 | GPIO9,SD_DATA2,SPIHD,HS1_DATA2,U1RXD |
| 18 | SWP/SD3 | GPIO10,SD_DATA3,SPIWP,HS1_DATA3,U1TXD |
| 19 | SCS/CMD | GPIO11,SD_CMD,SPICS0,HS1_CMD,U1RTS |
| 20 | SCK/CLK | GPIO6,SD_CLK,SPICLK,HS1_CLK,U1CTS |
| 21 | SDO/SD0 | GPIO7,SD_DATA0,SPIQ,HS1_DATA0,U2RTS |
| 22 | SDI/SD1 | GPIO8,SD_DATA1,SPID,HS1_DATA1,U2CTS |
| 23 | IO15 | GPIO15,ADC2_CH3,TOUCH3,MTDO,HSPICS0,RTC_GPIO13,HS2_CMD,SD_CMD , EMAC_RXD3 |
| 24 | IO2 | GPIO2,ADC2_CH2,TOUCH2,RTC_GPIO12,HSPIWP,HS2_DATA0,SD_DATA0 |
| 25 | IO0 | GPIO0,ADC2_CH1,TOUCH1,RTC_GPIO11,CLK_OUT1,EMAC_TX_CLK |
| 26 | IO4 | GPIO4,ADC2_CH0,TOUCH0,RTC_GPIO10,HSPIHD,HS2_DATA1, SD_DATA1, EMAC_TX_ER |
| 27 | IO16 | GPIO16,HS1_DATA4,U2RXD,EMAC_CLK_OUT |
| 28 | IO17 | GPIO17,HS1_DATA5,U2TXD,EMAC_CLK_OUT_180 |
| 29 | IO5 | GPIO5,VSPICS0,HS1_DATA6,EMAC_RX_CLK |
| 30 | IO18 | GPIO18,VSPICLK,HS1_DATA7 |
| 31 | IO19 | GPIO19,VSPIQ,U0CTS,EMAC_TXD0 |
| 32 | NC | - |
| 33 | IO21 | GPIO21,VSPIHD,EMAC_TX_EN |
| 34 | RXD0 | GPIO3,U0RXD,CLK_OUT2 |
| 35 | TXD0 | GPIO1,U0TXD,CLK_OUT3,EMAC_RXD2 |
| 36 | IO22 | GPIO22,VSPIWP,U0RTS,EMAC_TXD1 |
| 37 | IO23 | GPIO23,VSPID,HS1_STROBE |
| 38 | GND | Ground |

**Strapping Pin**

| Build-in LDO (VDD_SDIO)voltage | | | | | |
|---|---|---|---|---|---|
| Pin | Default | 3.3V | | 1.8V | |
| MTDI/GPIO12 | Pull down | 0 | | 1 | |
| System startup method | | | | | |
| Pin | Default | SPI Flash startup method | | Download startup method | |
| GPIO0 | Pull up | 1 | | 0 | |
| GPIO2 | Pull down | / | | 0 | |
| During system startup, U0TXD outputs log print information | | | | | |
| Pin | Default | U0TXD flip | | U0TXD static | |
| MTDO/GPIO15 | Pull up | 1 | | 0 | |
| SDIO slave signal input and output timing | | | | | |
| Pin | Default | Falling edge input Falling edge output | Falling edge input Rising edge output | Rising edge input Falling edge output | Rising edge input Rising edge output |
| MTDO/GPIO15 | Pull up | 0 | 0 | 1 | 1 |
| GPIO5 | Pull up | 0 | 1 | 0 | 1 |

**Note: ESP32 has a total of 6 strapping pins, software can read the value of these 6 bits in the register "GPIO_STRAPPING". During the chip power-on reset process, the strapping pin samples the level and stores it in the latch, which is latched as "0" or "1", and remains until the chip is powered down or turned off. Each strapping pin is connected to internal pull-up/pull-down. If a strapping pin is not connected or the connected external circuit is in a high impedance state, the internal weak pull-up/pull-down will determine the default value of the input level of the strapping pin. To change the value of the strapping bit, the user can apply an external pull-down/pull-up resistor, or use the GPIO of the host MCU to control the level of the strapping pin when the ESP32 is powered on and reset.**
**After reset, the strapping pin has the same function as the normal pin.**

# 3.Function description

## CPU and RAM

ESP32 contains two low-power Xtensa®32-bit LX6 MCUs. On-chip storage includes:

- 448KBytes ROM for program startup and kernel function call
- 520 KB on-chip SRAM for data and instruction storage
- 8KBytes of SRAM in RTC (RTC slow memory) can be accessed by the coprocessor in Deep-sleep mode
- The 8KBytes of SRAM in RTC, that is, RTC fast memory, can be used for data storage and accessed by the main CPU during RTC startup in Deep-sleep mode
- 1kbit EFUSE, of which 256 bits are dedicated to the system (MAC address and chip settings); the remaining 768 bits are reserved for user applications, which include Flash encryption and chip ID

## External Flash and SRAM

ESP32 supports up to four 16 MBytes external QSPI Flash and static random access memory (SRAM), and has a hardware encryption function based on AES to protect developers' programs and data.

- ESP32 accesses external QSPI Flash and SRAM through cache. Up to 16 MBytes of external Flash is mapped to the CPU code space, supporting 8-bit, 16-bit and 32-bit access, and executable code
- Up to 8M Bytes of external Flash and SRAM are mapped to the CPU data space, supporting 8-bit, 16-bit and 32-bit access. Flash only supports read operations, SRAM can support read and write operations

### Crystal oscillator

Supports crystal oscillators with frequencies of 40 MHz, 26 MHz and 24 MHz. The accuracy of the crystal oscillator is between ±10 PPM, and the operating temperature range is between -40° C and 85° C. Please select the correct crystal type when using the download tool. In the circuit design, the ground adjustment capacitors C1 and C2 are added to the input and output terminals of the crystal oscillator, respectively. The value of the two capacitors can be flexibly set, ranging from 6 pF to 22 pF. However, the specific capacitance value can only be determined after matching the overall performance of the entire circuit. Generally speaking, if the frequency of the crystal oscillator is 26 MHz, the capacitance values of C1 and C2 are within 10 pF; if the frequency of the crystal oscillator is 40 MHz, the capacitance values of C1 and C2 are 10 pF<C1, C2<22 pF. The frequency of the RTC crystal oscillator is usually 32 kHz or 32.768 kHz. Due to the internal calibration used to correct the frequency offset, the frequency of the crystal oscillator may exceed the range of ±20 PPM. When the chip is working in low-power mode, the device should select an external low-speed 32 kHz crystal oscillator clock instead of the internal RC oscillator to obtain an accurate wake-up time.

### Power consumption

ESP32 has advanced power management technology that can switch between various power saving modes.
Active mode: The chip's radio frequency is in working state. The chip can receive, transmit and listen to signals.
Modem-sleep mode: The CPU keeps running and the clock can be configured. Wi-Fi/Bluetooth baseband and radio frequency are turned off.
Light-sleep mode: The CPU is suspended. RTC and ULP coprocessors run. Any wake-up event (MAC, host, RTC timer or external interrupt) will wake up the chip.
Deep-sleep mode: Only RTC is working. Wi-Fi and Bluetooth connection data are stored in RTC. The ULP coprocessor keeps running.
Hibernation mode: The built-in 8 MHz oscillator and ULP coprocessor are both disabled. RTC memory recovery power is cut off. Only one RTC clock timer on the slow clock and certain RTC GPIOs are active. RTC timer or RTC GPIO can wake up the chip from Hibernation mode.
Associated sleep mode: The power saving mode can be switched between Active mode and Modem-sleep mode/Light-sleep mode. CPU,
Wi-Fi, Bluetooth, and radio frequency are periodically woken up as preset to ensure Wi-Fi/Bluetooth connection.
Ultra-low-power sensor monitoring mode: The main system is in Deep-sleep mode, and the ULP coprocessor is turned on or off periodically to measure sensor data. According to the data measured by the sensor, the ULP coprocessor decides whether to wake up the main system. The power consumption changes with the power saving mode/sleep mode and the working status of the functional module.

## 4. Electrical parameters

Unless otherwise specified, the test environment for the specifications listed in this chapter is：VBAT= 3.3V,TA= 27℃。

### Limit parameters：

| Rated value | Condition | Value | Unit |
|---|---|---|---|
| Storage temperature | - | -40~85 | ℃ |
| Maximum welding temperature | - | 260 | ℃ |
| Supply voltage | IPC/JEDEC J-STD-020 | +3.0~+3.6 | V |

### Recommended working conditions：

| Working environment | Name | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|
| Operating | - | -40 | 20 | 85 | ℃ |

| | | | | | |
|---|---|---|---|---|---|
| temperature | | | | | |
| Supply voltage | VDD | 3.0 | 3.3 | 3.6 | V |

## Digital port characteristics:

| Port | Name | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|
| Input logic level is low | VIL | -0.3 | - | 0.25VDD | V |
| Input logic level is high | | 0.75VDD | - | VDD+0.3 | V |
| Out put logic level is low | VOL | N | - | 0.1VDD | V |
| Output logic level is high | | 0.8VDD | - | N | V |

## Wi-Fi RF characteristics:

| Description | Min | Typical value | Max | Unit |
|---|---|---|---|---|
| General features | | | | |
| Input frequency | 2412 | - | 2484 | MHz |
| Input resistance | - | 50 | - | Ω |
| Input launch | - | - | -10 | dB |
| PA output power | 15.5 | 16.5 | 21.5 | dBm |
| Sensitivity | | | | |
| DSSS,1Mbps | - | -98 | - | dBm |
| CCK, 11 Mbps | - | -90 | - | dBm |
| OFDM, 6 Mbps | - | -93 | - | dBm |
| OFDM, 54 Mbps | - | -75 | - | dBm |
| HT20, MCSO | - | -93 | - | dBm |
| HT20, MCS7 | - | -73 | - | dBm |
| HT40, MCSO | - | -90 | - | dBm |
| HT40, MCS7 | - | -70 | - | dBm |
| MCS32 | - | -91 | - | dBm |
| Adjacent Channel Suppression | | | | |
| OFDM, 6 Mbps | - | 37 | - | dB |
| OFDM, 54 Mbps | - | 21 | - | dB |
| HT20, MCS0 | - | 37 | - | dB |
| HT20, MCS7 | - | 20 | - | dB |

## BLE receiver features:

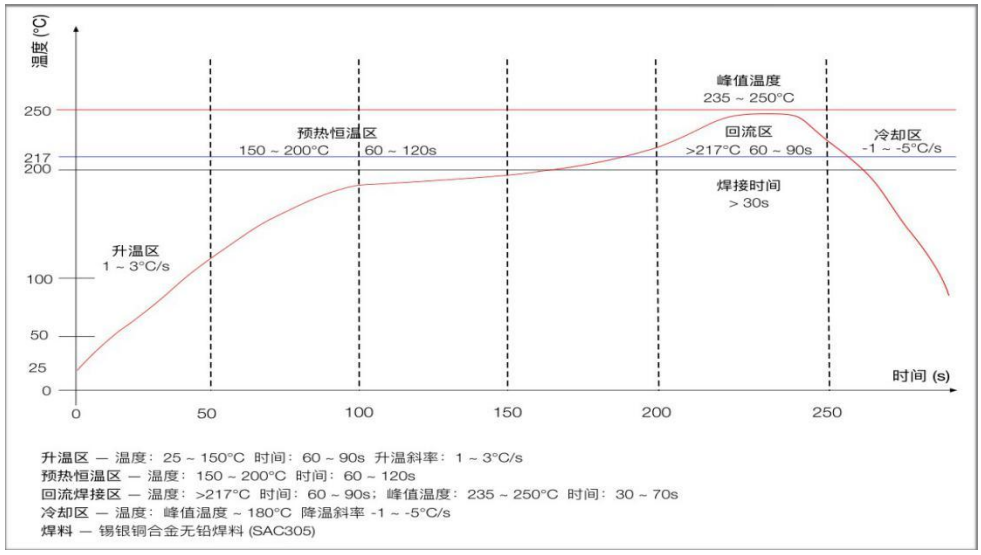
| Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|
| Sensitivity@ 0.1% BER | - | - | -98 | - | dBm |
| Max received signal@0.1% BER | - | 0 | - | - | dBm |
| Co-channel C/I | - | - | +10 | - | dB |
| Adjacent channel selectivity C/I | F = F0 + 1 MHz | - | -5 | - | dB |
| | F = F0 - 1 MHz | - | -5 | - | dB |
| | F = F0 + 2 MHz | - | -25 | - | dB |
| | F = F0 - 2 MHz | - | -35 | - | dB |
| | F = F0 + 3 MHz | - | -25 | - | dB |
| | F = F0 - 3 MHz | - | -45 | - | dB |
| Out-of-band blocking | 30MHz-2000MHz | -10 | - | - | dBm |
| | 2000MHz-2400MHz | -27 | - | - | dBm |

| | | | | | |
|---|---|---|---|---|---|
| performance | 2500MHz-3000MHz | -27 | - | - | dBm |
| | 3000MHz-12.5GHz | -10 | - | - | dBm |
| Intermodulation performance | - | -36 | - | - | dBm |

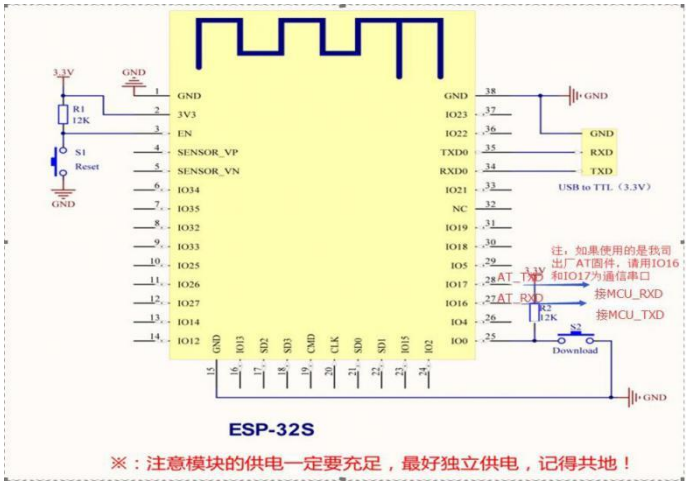
## BLE transmitter characteristics:

| Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|
| RF transmit frequency | - | - | +7.5 | +10 | dBm |
| RF power control range | - | - | 25 | - | dB |
| Adjacent channel transmit power | F = F0 + 1 MHz | - | -14.6 | - | dBm |
| | F = F0 - 1 MHz | - | -12.7 | - | dBm |
| | F = F0 + 2 MHz | - | -44.3 | - | dBm |
| | F = F0 - 2 MHz | - | -38.7 | - | dBm |
| | F = F0 + 3 MHz | - | -49.2 | - | dBm |
| | F = F0 - 3 MHz | - | -44.7 | - | dBm |
| | F = F0 + > 3 MHz | - | -50 | - | dBm |
| | F = F0 - > 3 MHz | - | -50 | - | dBm |
| Δf1avg | - | - | - | 265 | kHz |
| Δf2max | - | 247 | - | - | kHz |
| Δf2avg/Δf1avg | - | - | -0.92 | - | - |
| ICFT | - | - | -10 | - | kHz |
| Frequency drift rate | - | - | 0.7 | - | kHz/50us |
| Frequency drift | - | - | 2 | - | kHz |

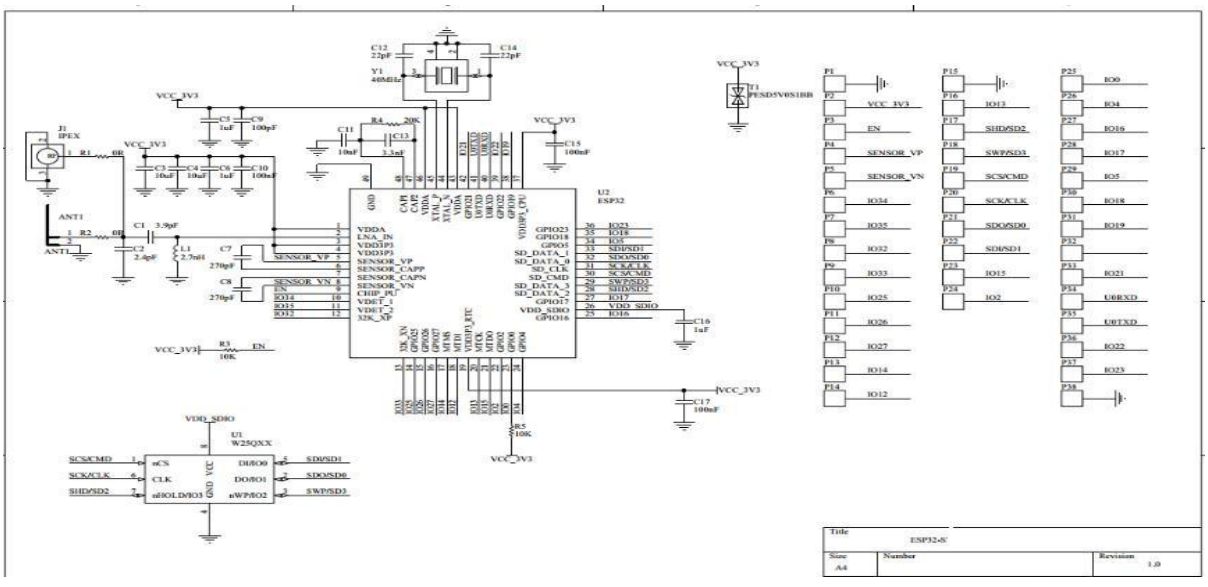
## 5. Reflow soldering curve




## 6. Application circuit




## 7. Schematic diagram



# 8. Contact us

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