SPECIFICATION

Product Type	:	EPD
Description	:	Screen Size: 2.13" Color: Black and White Display Resolution: 250*122
Issue Date	:	2017.03.02

Waveshare Electronics
10F, International Science &
Technology Building, Fuhong Rd,
Futian District, Shenzhen, China

Version	Content	Date	Producer
1.0	New release	Jul.15.2014	
1.1	Update resolution	Jan.19.2015	
1.2	Update software setting	Mar.26.2015	
1.3	Add packing notes	May.18.2015	
2.0	Modify Reference Circuit	Mar.02.2017	

CONTENTS

1. General Description

This display is an Active Matrix Electrophoretic Display(AMEPD) , with interface and a reference system design. The 2.13" active area contains 122×250 pixels, and has 1-bit full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM. LUT ,VCOM, and border are supplied with each panel.

2. Features

122x250 pixels display
White reflectance above 35%
Contrast ratio above 8:1
Ultra wide viewing angle
Ultra low power consumption
Pure reflective mode
Bi-stable display
Commercial temperature range
Landscape, portrait modes
Hard-coat antiglare display surface
Ultra Low current deep sleep mode
On chip display RAM
Waveform stored in On-chip OTP
Serial peripheral interface available
On-chip oscillator
On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
I^2C signal master interface to read external temperature sensor

3. Application

Electronic Shelf Label System

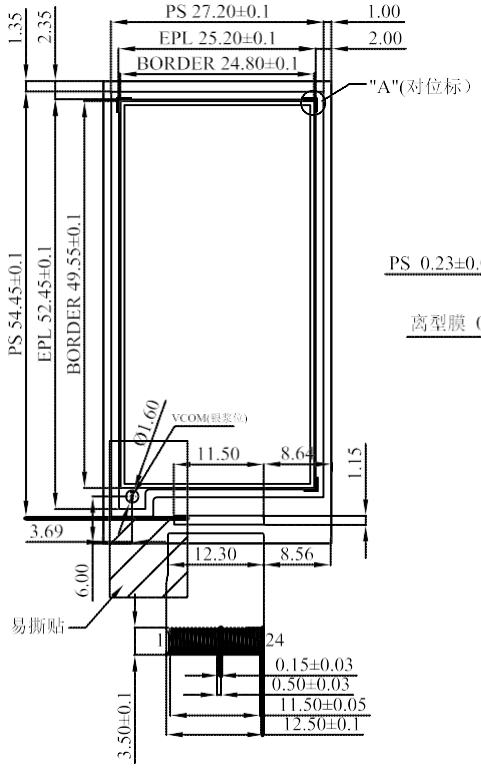
4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	122(H)x250(V)	Pixel	
Active Area	23.71(H)×48.55(V)	mm	
Pixel Pitch	0.194×0.194	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.2(H)×59.2 (V) ×1.05(D)	mm	
Weight	3.5±0.5	g	

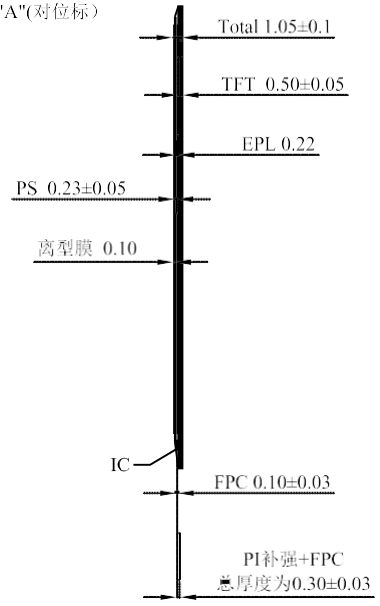
已确认此版本的所有图纸			
签名:		日期:	

REV.:	DESCRIPTION	DATE
A0	初始版本	14.08.25

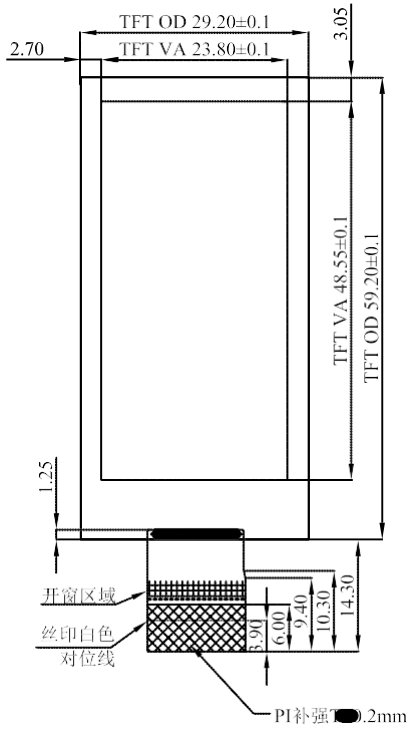
FRONT VIEW



SIDE VIEW



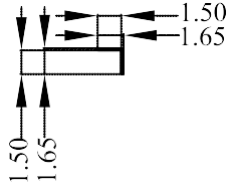
BOTTOM VIEW



PIN	SIGNAL
1	NC
2	GDR
3	RESE
4	VGL
5	VGH
6	TSCL
7	TSDA
8	BS1
9	BUSY
10	RES#
11	D/C#
12	CS#
13	D0
14	D1
15	VDDIO
16	VCI
17	VSS
18	VDD
19	VPP
20	VSH
21	PREVGH
22	VSL
23	PREVGL
24	VCOM

NOTES:

1. DISPALY MODE 2.13" ARREY FOR EPD;
2. DRIVE IC:
3. RESOLUTION:250gate X 122source;
4. pixel size:0.1942mm X 0.1943mm;
5. Unspecified Tolerance:±0.20;
6. Material conform to the ROHS standard



"A"(2:1)

WAVESHARE CO., LTD

ALL UNITS: mm	DATE	MODEL NUMBER :		SHEET: 1
DWN: W.R.P	14.08.25			
CHK: W.A.M		CUSTOMER NO.:		DATE: 14.08.31
APP: J.Y.C		P/N	PROJECTION	

6. Input/Output Terminals

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	-	NC	No connection and do not connect with other NC pins	
7	O	TOUT1	Serial data pin for panel break detection	
8	I	BS1	Bus selection pin	Note 6-5
9	O	BUSY	Busy state output pin	Note 6-4
10	I	RES #	Reset	Note 6-3
11	I	D/C #	Data /Command control pin	Note 6-2
12	I	CS #	Chip Select input pin	Note 6-1
13	I/O	D0 (SCLK)	serial clock pin (SPI)	
14	I/O	D1 (SDIN)	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Positive Gate driving voltage	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH,the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is Low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

7. MCU Interface

7.1 MCU interface selection

The IL3895 can support 3-wire/4 serial peripheral interface. In the IL3895, the MCU interface is pin selectable by BS1 pins shown in.

Table 7-1: MCU interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) - 9 bits SPI

7.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C# and CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-1 and the write procedure 4-wire SPI is shown in 错误！未找到引用源。

Table 7-1 : Control pins status of 4-wire SPI

Function	D0 (SCLK) pin	D1 (SDIN) pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

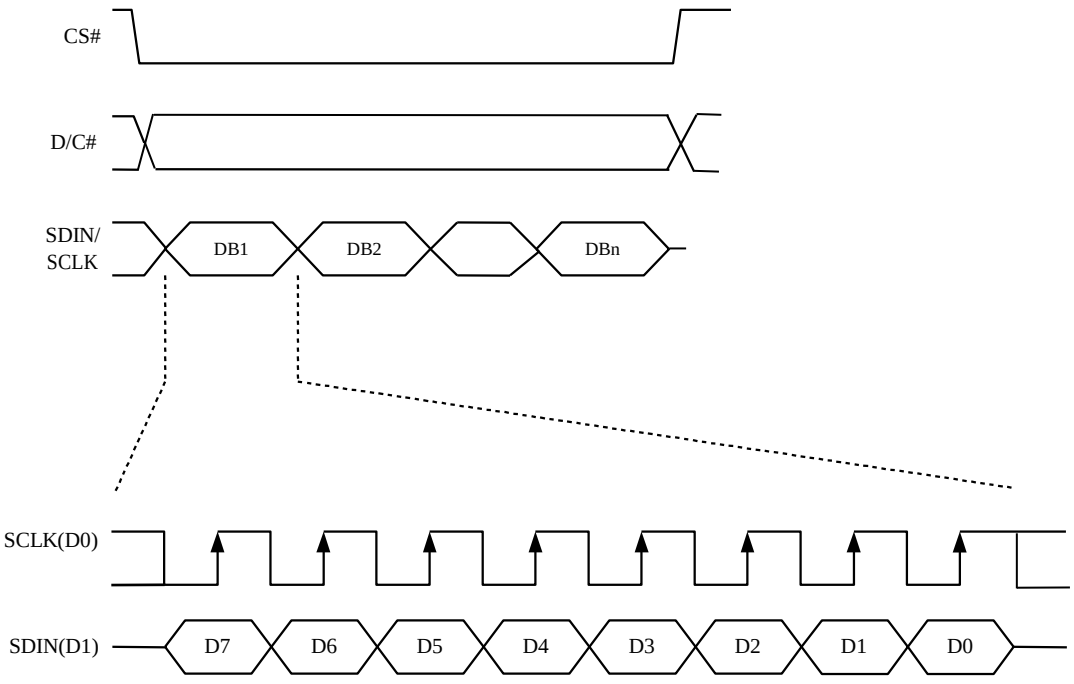
Note:

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

(3) SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

Figure 7-1 : Write procedure in 4-wire SPI



7.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCLK, serial data SDIN and CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-2.

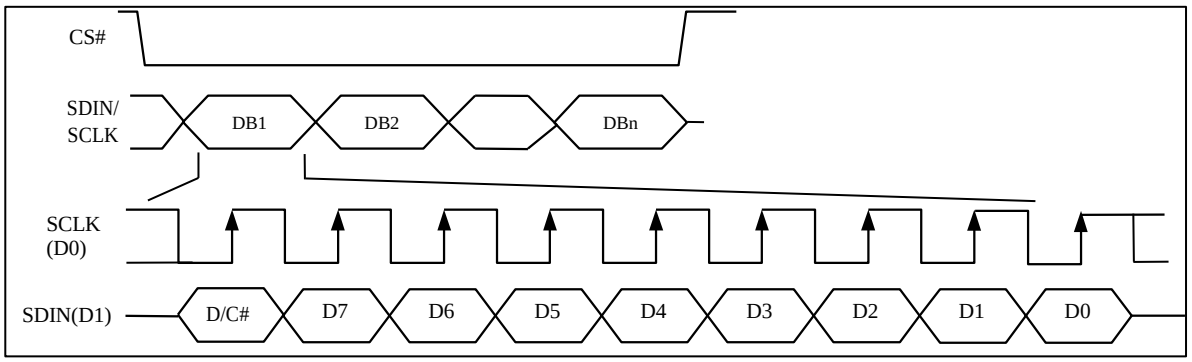
In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Figure 7-2 shows the write procedure in 3-wire SPI

Table 7-2 : Control pins status of 3-wire SPI

Function	SCLK pin	SDIN pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:
(1)L is connected to V_{SS} and H is connected to V_{DDIO}
(2)↑ stands for rising edge of signal

Figure 7-2 : Write procedure in 3-wire SPI



8. Temperature Register Mapping

1. If the Temperature value MSByte bit D11 = 0, then

The temperature is positive and value (DegC) = + (Temperature value) / 16

2. If the Temperature value MSByte bit D11 = 1, then

The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

9. Panel Break Detection

The panel break detection function is used to detect the breakage at panel edge. When the panel break detection command is issued, the panel break detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of panel break.

10. COMMAND TABLE

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="3">Driver Output Control</td><td rowspan="3">Set the number of gate. Setting for 232 gates is:
Set A[7:0] = F9h
Set B[7:0] = 00h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="3">Gate Driving Voltage Control</td><td rowspan="3">Set Gate driving voltage.
A[4:0] = 10h [POR], VGH at 22V
B[3:0] = 0Ah [POR], VGL at -20V</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Source Driving voltage Control</td><td rowspan="2">Set Source output voltage.
A[4:0] = 19h [POR], VSH/VSL at +/-15V</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep Mode</td><td>Deep Sleep mode Control</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A0</td><td><table><tr><td>A[0]</td><td>Description</td></tr><tr><td>0</td><td>Normal Mode [POR]</td></tr><tr><td>1</td><td>Enter Deep Sleep Mode</td></tr></table></td></tr>
<tr><td>0</td><td>0</td><td>11</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Data Entry mode setting</td><td rowspan="2">Define data entry sequence.

A [1:0] = ID[1:0]
Address automatic increment / decrement setting
The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.
00 – Y decrement, X decrement,
01 – Y decrement, X increment,
10 – Y increment, X decrement,
11 – Y increment, X increment [POR]

A[2] = AM
Set the direction in which the address counter is updated automatically after data is written to the RAM.
When AM= 0, the address counter is updated in the X direction. [POR]
When AM = 1, the address counter is updated in the Y direction.

Remark: More information in section 6.1</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>SWRESET</td><td>It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode
Note: RAM are unaffected by this commad.</td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="3">Temperature Sensor Control (Write to temperature register)</td><td rowspan="3">Write to temperature register.
A[7:0] – MSByte 01111111[POR]
B[7:0] – LSByte 11110000[POR]

Remark: More information in section 6.2.</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence.

The Display Update Sequence Option is located at R22h

User should not interrupt this operation to avoid corruption of panel images.</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Display Update Control 1</td><td>Option for Display Update
Bypass Option used for Pattern Display, which is used for display the RAM content into the Display

OLD RAM Bypass option
A [7]
A[7] = 1: Enable bypass
A[7] = 0: Disable bypass [POR]

A[4] value will be used as New RAM for bypass.
A[4] = 0 [POR]

A[1:0] Initial Update Option - Source Control
<table><tr><th>A[1:0]</th><th>GSA</th><th>GSB</th></tr><tr><td>01[POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td>Display Update Sequence Option:
Enable the stage for Master Activation
<table><tr><th></th><th>Parameter (in Hex)</th></tr><tr><td>Enable Clock Signal,
Then Enable Analog
Then Load LUT
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>FF
[POR]</td></tr><tr><td><u>Setting for LUT from OTP</u>
Enable Clock Signal,
Then Enable Analog
Then Load LUT
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>D7</td></tr><tr><td><u>Setting for LUT from MCU</u>
Enable Clock Signal,
Then Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>C7</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>23</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Panel Break Detection</td><td>After this command is issued, panel break detection will start. The status can be checked by Command 2Fh. During detection, BUSY pad will output high. The command required CLKEN=1.</td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM</td><td>After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Write VCOM register</td><td>Write VCOM register from MCU interface
<table>
<tr><th>A[7:0]</th><th>VCOM (V)</th><th>A[7:0]</th><th>VCOM (V)</th></tr>
<tr><td>0Fh</td><td>-0.2</td><td>5Ah</td><td>-1.7</td></tr>
<tr><td>14h</td><td>-0.3</td><td>5Fh</td><td>-1.8</td></tr>
<tr><td>19h</td><td>-0.4</td><td>64h</td><td>-1.9</td></tr>
<tr><td>1Eh</td><td>-0.5</td><td>69h</td><td>-2</td></tr>
<tr><td>23h</td><td>-0.6</td><td>6Eh</td><td>-2.1</td></tr>
<tr><td>28h</td><td>-0.7</td><td>73h</td><td>-2.2</td></tr>
<tr><td>2Dh</td><td>-0.8</td><td>78h</td><td>-2.3</td></tr>
<tr><td>32h</td><td>-0.9</td><td>7Dh</td><td>-2.4</td></tr>
<tr><td>37h</td><td>-1</td><td>82h</td><td>-2.5</td></tr>
<tr><td>3Ch</td><td>-1.1</td><td>87h</td><td>-2.6</td></tr>
<tr><td>41h</td><td>-1.2</td><td>8Ch</td><td>-2.7</td></tr>
<tr><td>46h</td><td>-1.3</td><td>91h</td><td>-2.8</td></tr>
<tr><td>4Bh</td><td>-1.4</td><td>96h</td><td>-2.9</td></tr>
<tr><td>50h</td><td>-1.5</td><td>9Bh</td><td>-3</td></tr>
<tr><td>55h</td><td>-1.6</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>0</td><td>0</td><td>2F</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Status Bit Read</td><td rowspan="2">A[3] : Panel-Break flag (POR=0)
0:Normal
1:Broken
A[1:0] : Chip ID (POR=01)</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>0</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>32</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="5">Write LUT register</td><td rowspan="5">Write LUT register from MCU interface [30 bytes]
(excluding the VSH/VSL and Dummy bit)</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Set dummy line period</td><td rowspan="2">Set A[7:0] = 06h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Set Gate line width</td><td rowspan="2">Set A[3:0] = 0Bh</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td rowspan="2">Select border waveform for VBD
A[7] Follow Source at Initial Update Display
A [7]=0: [POR]
A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE.
A [6] Select GS Transition/ Fix Level for VBD
A [6]=0: Select GS Transition A[3:0] for VBD
A [6]=1: Select FIX level Setting A[5:4] for VBD [POR]
A [5:4] Fix Level Setting for VBD
<table>
<tr><th>A[5:4]</th><th>VBD level</th></tr>
<tr><td>00</td><td>VSS</td></tr>
<tr><td>01</td><td>VSH</td></tr>
<tr><td>10</td><td>VSL</td></tr>
<tr><td>11[POR]</td><td>HiZ</td></tr>
</table>
A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0])
<table>
<tr><th>A[1:0]</th><th>GSC</th><th>GSD</th></tr>
<tr><td>01[POR]</td><td>GS0</td><td>GS1</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: X-Start, POR = 00h B[4:0]: X-End, POR = 12h
0	1	-	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1	-	0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[7:0]: Y-Start, POR = 00h B[7:0]: Y-End, POR = F9h
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1	-	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X - address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0] : POR is 00h
0	1	-	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y - address counter	Make initial settings for the RAM Y address in the address counter (AC) A[7:0] : POR is 00h
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

11. ABSOLUTE MAXIMUM RATING

Table 11-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	0 to 40	°C
T_{STG}	Storage temperature range	-10 to 50	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI be constrained to the range VSS < VCI. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12.DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR}=25℃.

Table 12-1: DC Characteristics

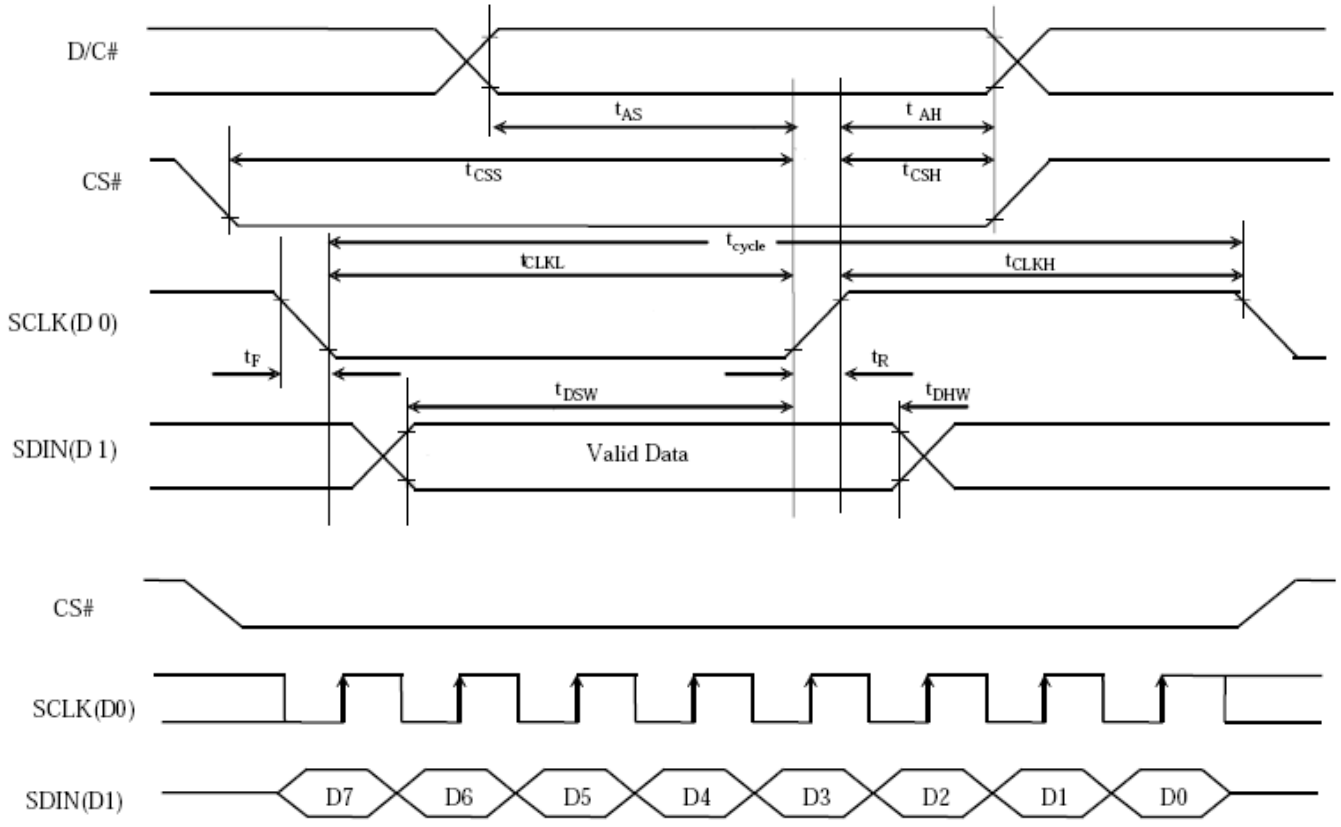
Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{CI}	VCI operation voltage		VCI	2.4	3.0	3.7	V
V_{IH}	High level input voltage		D1 (SDIN), D0 (SCLK), CS#, D/C#, RES#, BS1	$0.8V_{DDIO}$			V
V_{IL}	Low level input voltage					$0.2V_{DDIO}$	V
V_{OH}	High level output voltage	IOH = -100uA	BUSY, TOUT1	$0.9V_{DDIO}$			V
V_{OL}	Low level output voltage	IOL = 100uA				$0.1V_{DDIO}$	V

13. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.4V to 3.7V, T_{OPR}=25℃

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Figure 13-1 : Serial peripheral interface characteristics



13.3 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	-	26.4	40	mW	-
Power consumption in standby mode	-	-	-	0.017	mW	-

14. Reference Circuit

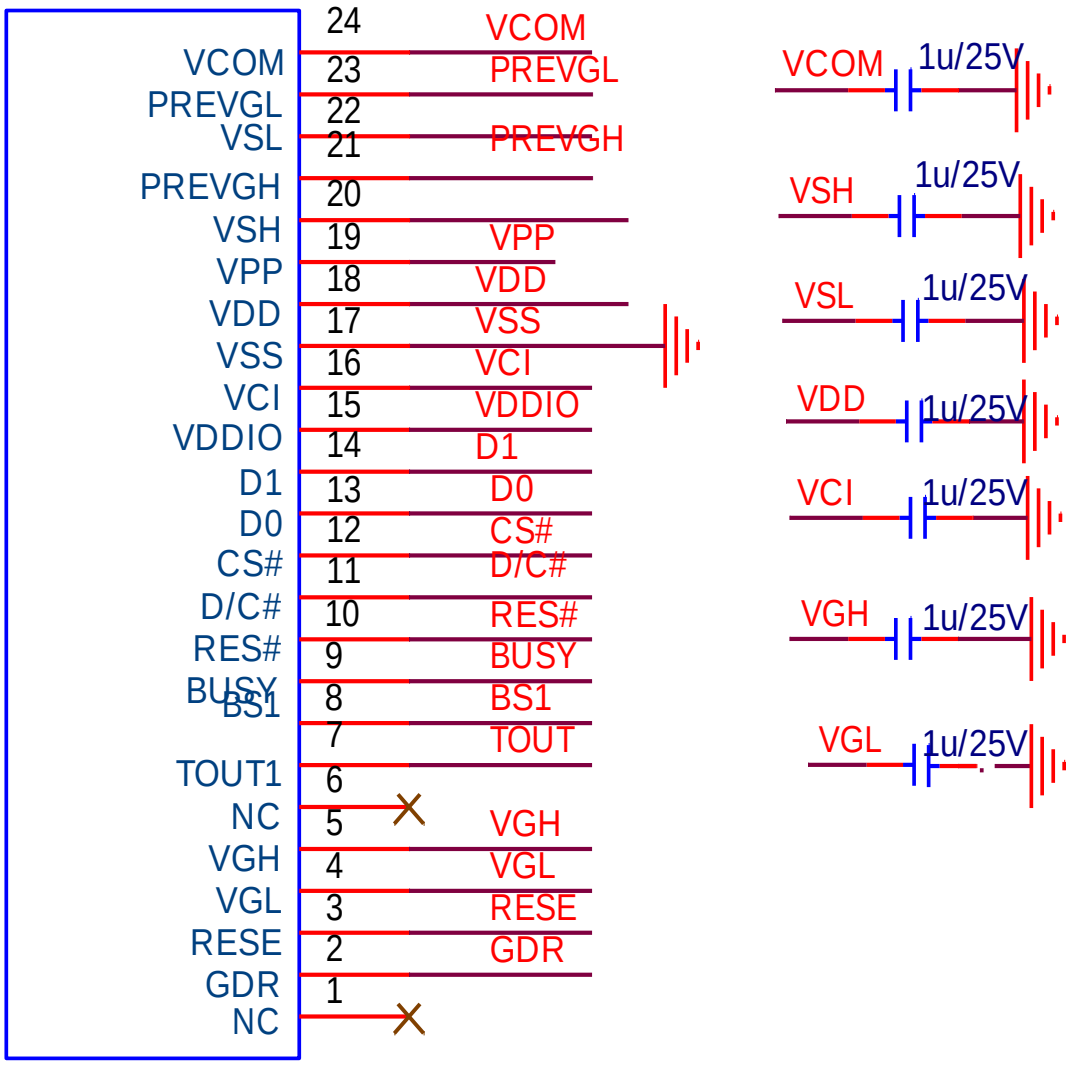


Figure . 14-1

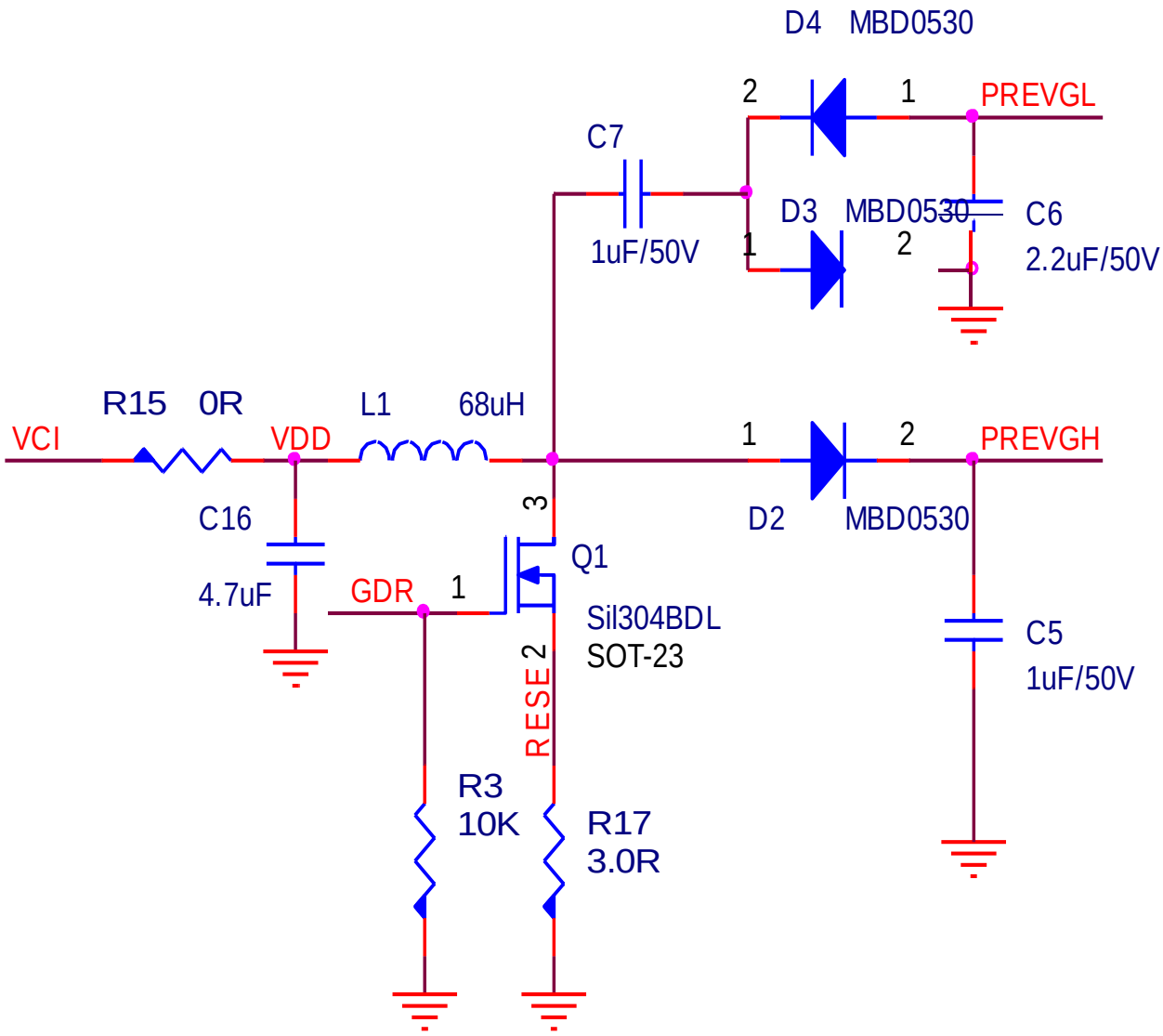
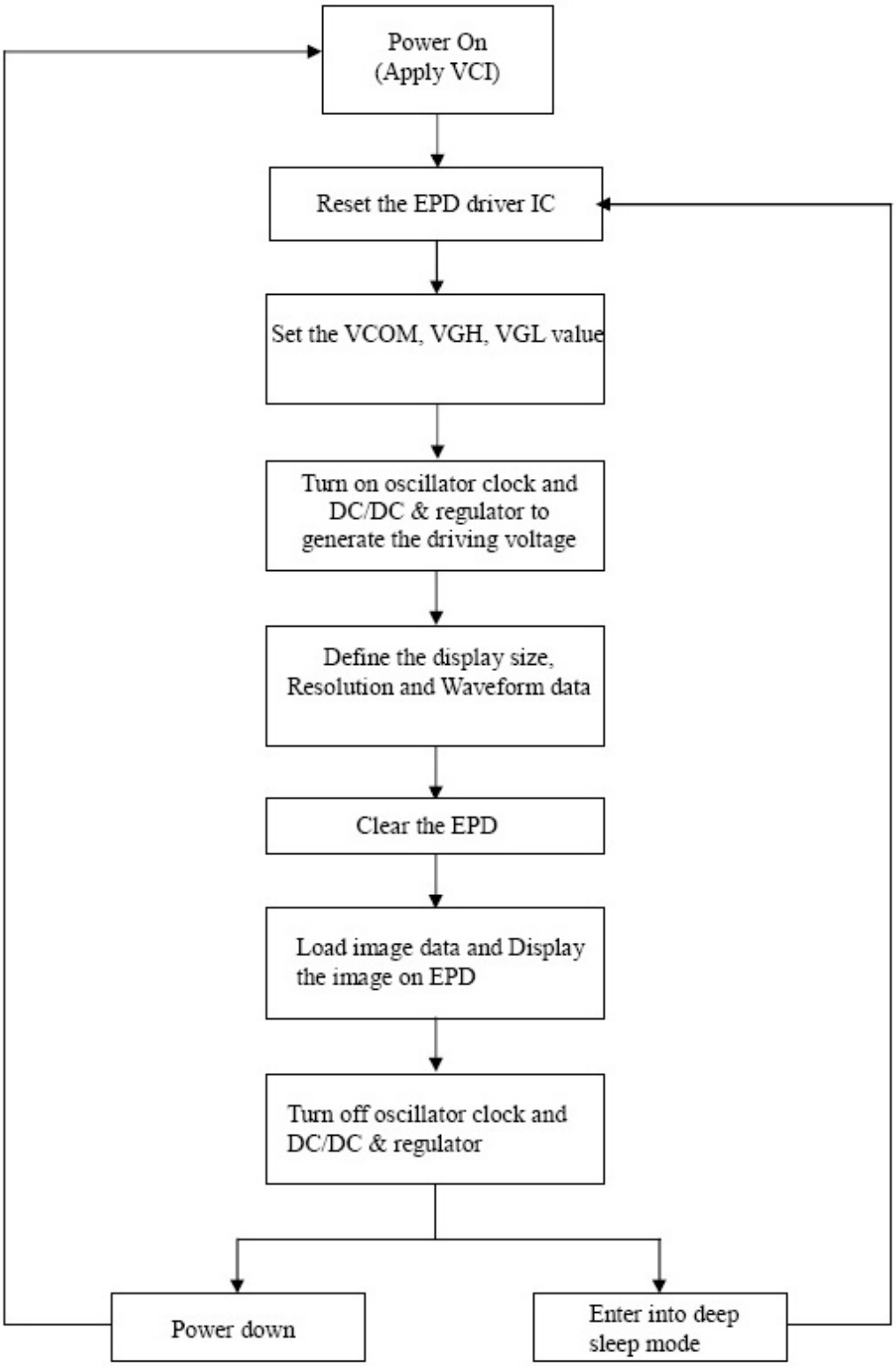

D4 MBD0530
2
1
PREVGL
C7
1uF/50V
D3 MBD0530
1
2
C6
2.2uF/50V
R15 0R
L1 68uH
VCI
VDD
1
2
PREVGH
C16
4.7uF
3
Q1
D2 MBD0530
GDR
1
Sil304BDL
SOT-23
C5
1uF/50V
RESE 2
R3
10K
R17
3.0R

Figure . 14-3

15. Typical Operating Sequence

15.1 Normal Operation Flow



16. Optical characteristics

16.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	34	-	%	Note 17-1
Gn	2Grey Level	-	-	DS+(WS-DS) xn (m-1)	-	L*	-
CR	Contrast Ratio	indoor	7		-	-	-
T_{update}	Update time	25℃	-	680ms	-	sec	-
Panel's life		0℃~40℃		1000000 times or 5 years			Note 17-2

WS : White state, DS : Dark state

Gray state from Dark to White : DS、WS

m : 2

Note 17-1 : Luminance meter : Eye - One Pro Spectrophotometer

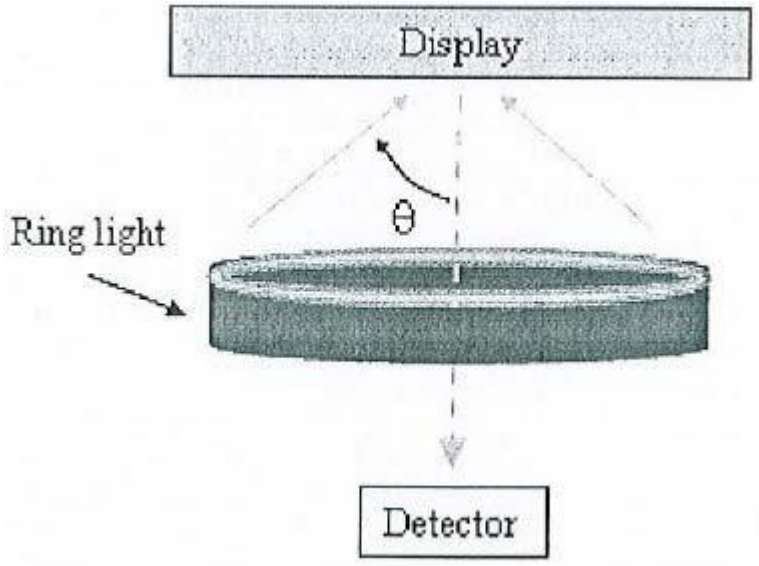
Note 17-2 :When work in temperature below 0 degree or above 40 degree , we do not recommend because the panel's life will not be guaranteed

16.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

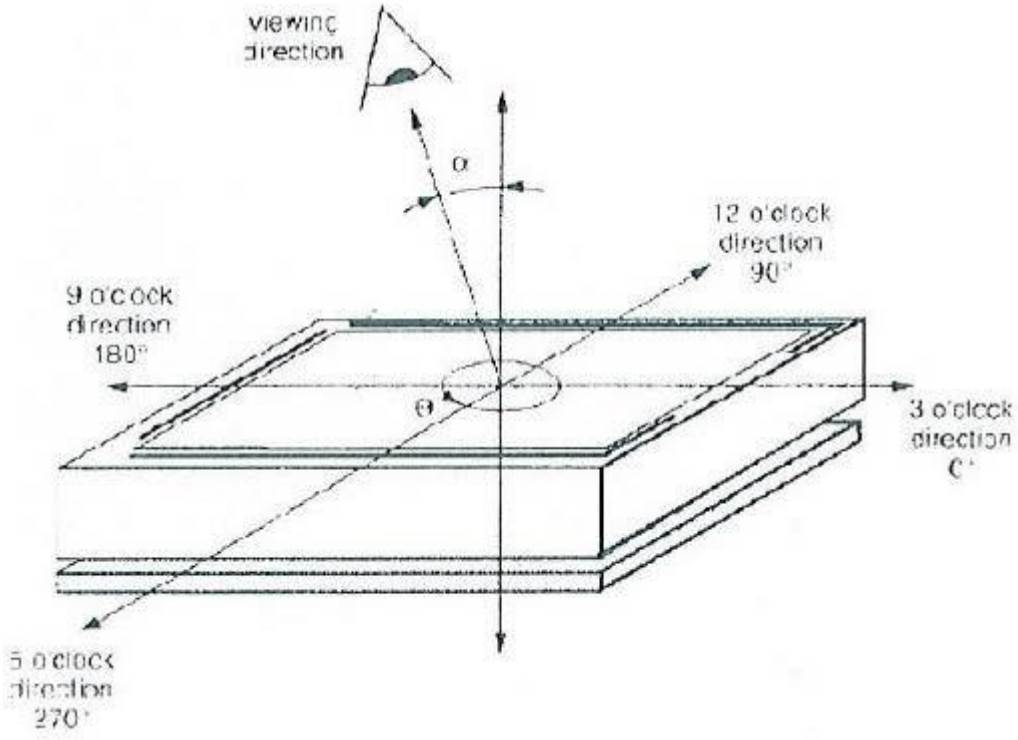


16.3 Reflection Ratio

The reflection ratio is expressed as :

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1) . $L_{\text{white board}}$ is the luminance of a standard white board . Both are measured with equivalent illumination source . The viewing angle shall be no more than 2 degrees .



16.4 Bi-stability

The Bi-stability standard as follows:

Bi-stability	Result		
24 hours Luminance drift		AVG	MAX
	White state ΔL*	-	3
	Black state ΔL*	-	3

17. HANDLING,SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface . Handle with care.Should the display break, do not touch the electrophoretic material . In case of contact with electrophoretic material ,wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases , such as acid and alkali gases , which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components . The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied . Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given , it is advisory and dose not form part of the specification.	
Product Environmental certification	
ROHS	

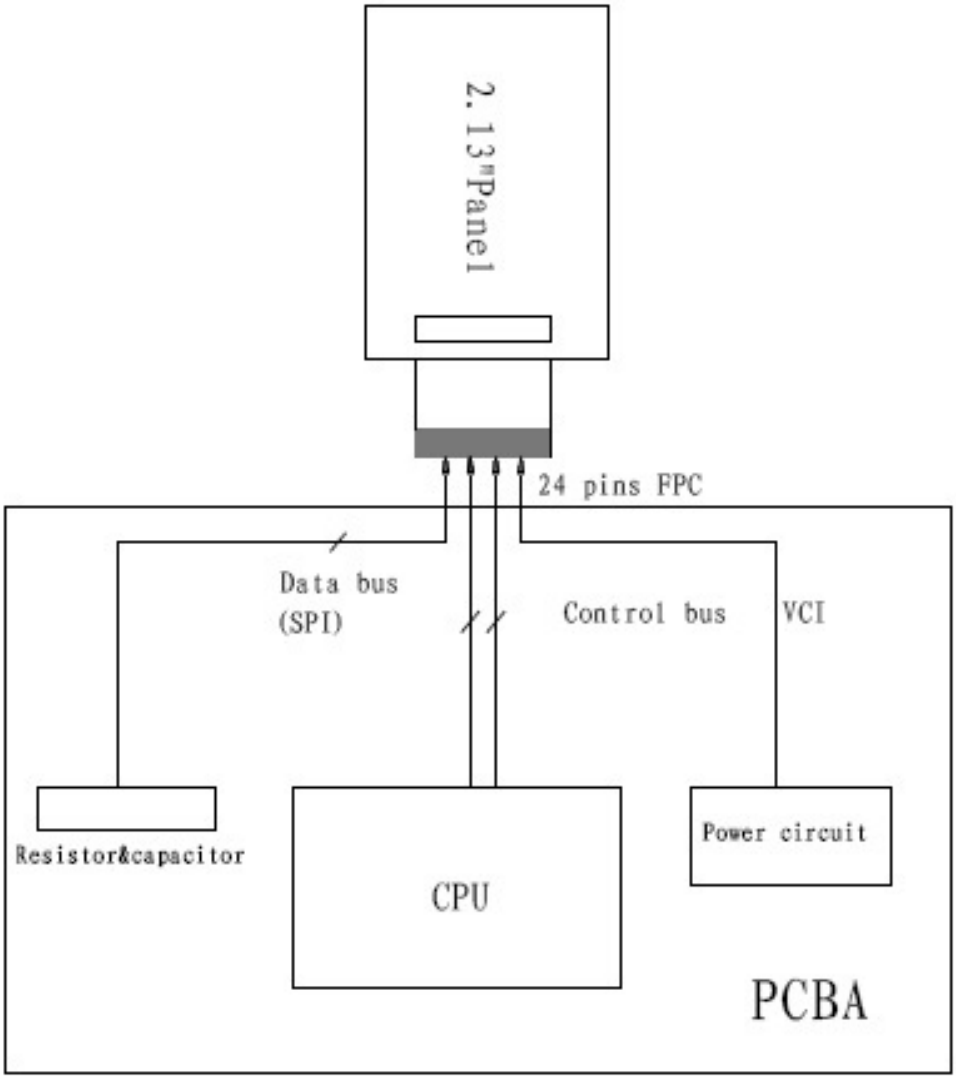
18. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 50℃,30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0℃for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70℃,23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25℃for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=+40℃,RH=90%for 240hrs	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=+60℃,RH=80%for 240hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	[-25℃30mins]→ [+70℃30mins] ,1000cycles Test in white pattern	IEC 60 068-2-14NB	

Actual EMC level to be measured on customer application.

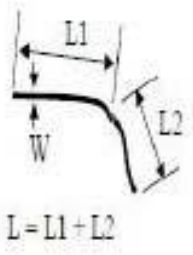
Note : The protective film must be removed before temperature test.

19. Block Diagram

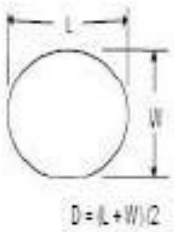


20. Point and line standard

<table>
<tr><td colspan="7">Shipment Inseption Standard</td></tr>
<tr><td colspan="7">Equipment：Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline demension：
36.7(H)×79.0(V) ×1.05(D)</td><td colspan="2"></td><td colspan="2"></td><td>Unit：㎜</td><td></td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>19℃～25℃</td><td>40%～55%RH</td><td>700～1000Lux</td><td>200～400 ㎜</td><td>35Sec</td><td></td></tr>
<tr><td rowspan="11">appearance standard</td><td>Defet type</td><td>Inspection</td><td colspan="2">Standard</td><td>Part-A</td><td></td></tr>
<tr><td rowspan="2">dead/
switch point</td><td rowspan="3">Electric Display</td><td colspan="2">D≤0.2 ㎜</td><td>Ignore</td><td rowspan="2"></td></tr>
<tr><td colspan="2">0.2 ㎜＜D≤0.4 ㎜</td><td>N≤3</td></tr>
<tr><td>（point overproof）</td><td colspan="2">D＞0.4 ㎜</td><td>Not Allow</td><td></td></tr>
<tr><td rowspan="2">2.line (no switch)</td><td rowspan="2">Electric Display</td><td colspan="4">L≤0.5mm, to point to determine</td></tr>
<tr><td colspan="4">L≤4W, to point to determine</td></tr>
<tr><td>3.line
（Switching line）</td><td>Electric Display</td><td colspan="4">Ignore in gray scale viewing
In Blak&white viewing Follow Non-Switching Criteria</td></tr>
<tr><td>4.Display unwork</td><td>Electric Display</td><td colspan="4">Not Allow</td></tr>
<tr><td>5.Display error</td><td>Electric Display</td><td colspan="4">Not Allow</td></tr>
<tr><td>6.warping</td><td>Vsual</td><td colspan="4">T<0.5mm，Ignore；</td></tr>
<tr><td rowspan="3">7.Protector hurt</td><td rowspan="3">Vsual</td><td colspan="4">L≤2 ㎜，W≤0.05 ㎜，Ignore；</td></tr>
<tr><td colspan="4">0.05mm＜W≤0.1mm，L≤4mm, N≤2</td></tr>
<tr><td colspan="4">L＞4 ㎜，W＞0.1 ㎜，Not Allow；</td></tr>
<tr><td rowspan="3">8.PS Bubble</td><td rowspan="3">Vsual</td><td colspan="4">D≤0.20mm, Ignore；</td></tr>
<tr><td colspan="4">0.2mm≤D＜0.35mm & N≤2</td></tr>
<tr><td colspan="4">D＞0.35 mm，Not Allow；</td></tr>
<tr><td>9.Packing</td><td>Vsual</td><td colspan="4">cannot be dirty and breakdown;must be marked and identified</td></tr>
<tr><td rowspan="2">Remark</td><td colspan="6">1.Cannot be defect&failure cause by appearence defect；</td></tr>
<tr><td colspan="6">2.Cannot be larger size cause by appearence defect；</td></tr>
</table>



Line Defect



Spot Defect

L=long W=wide D=point size

Edition	Content	Date
1	New edition	Sep.26.2014